VR-Scale: Runtime Dynamic Phase Scaling of Processor VRs for Improving Power Efficiency

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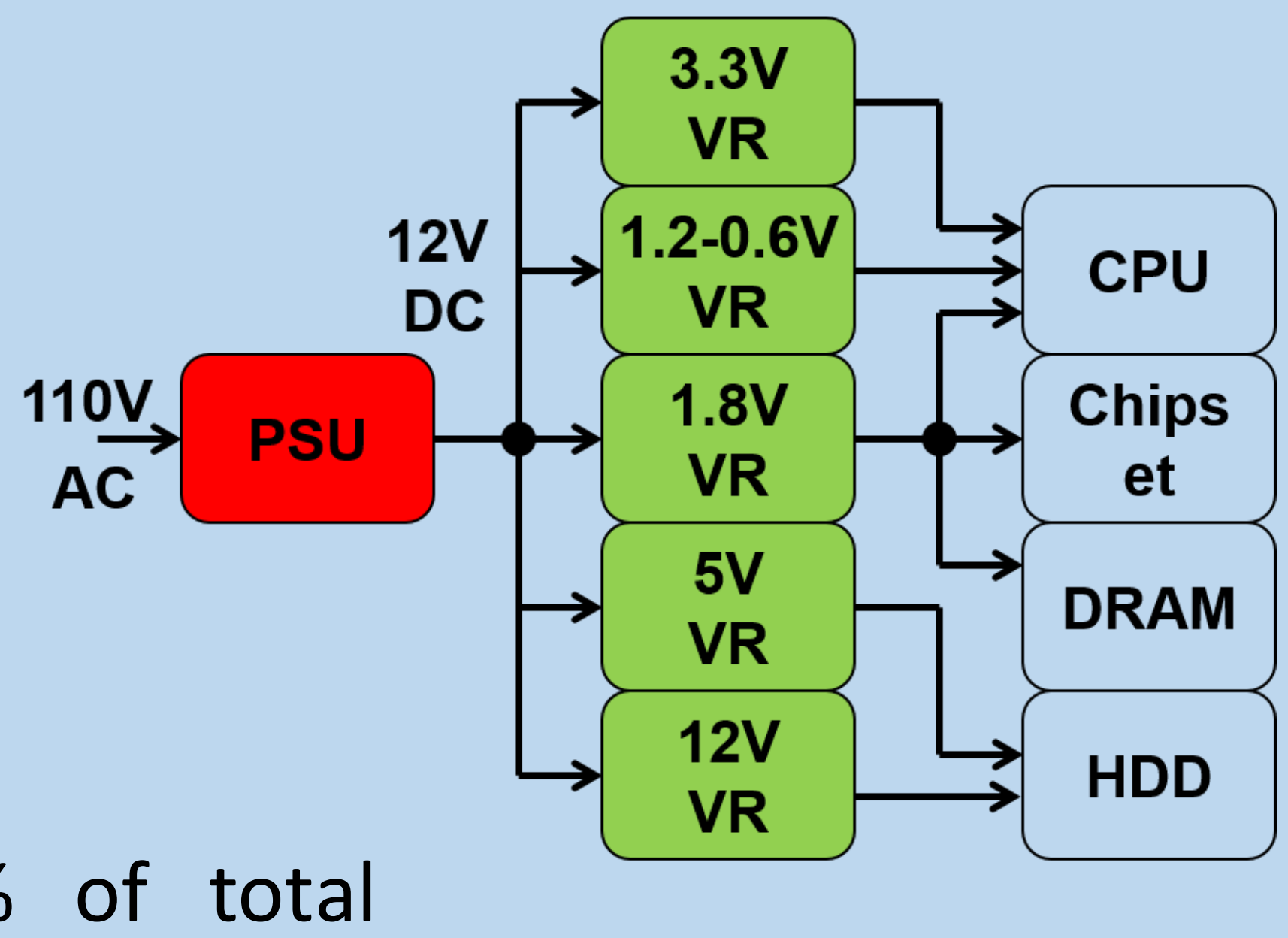
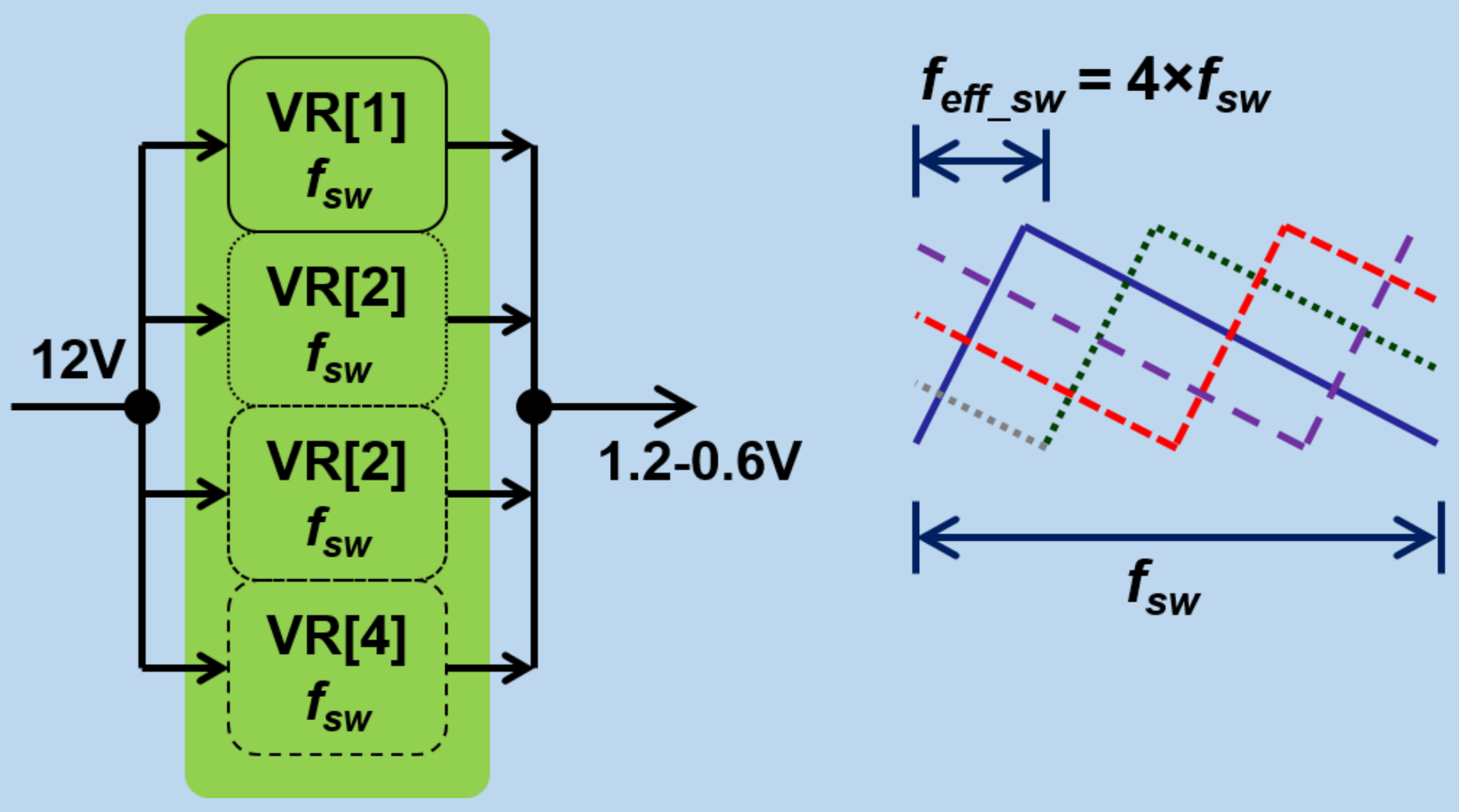
Motivation

- For the system power delivery, the AC voltage is transformed to DC voltage through PSU. Then, there are multiple VR modules to scale the voltage level for each specific module such as CPU, DRAM.



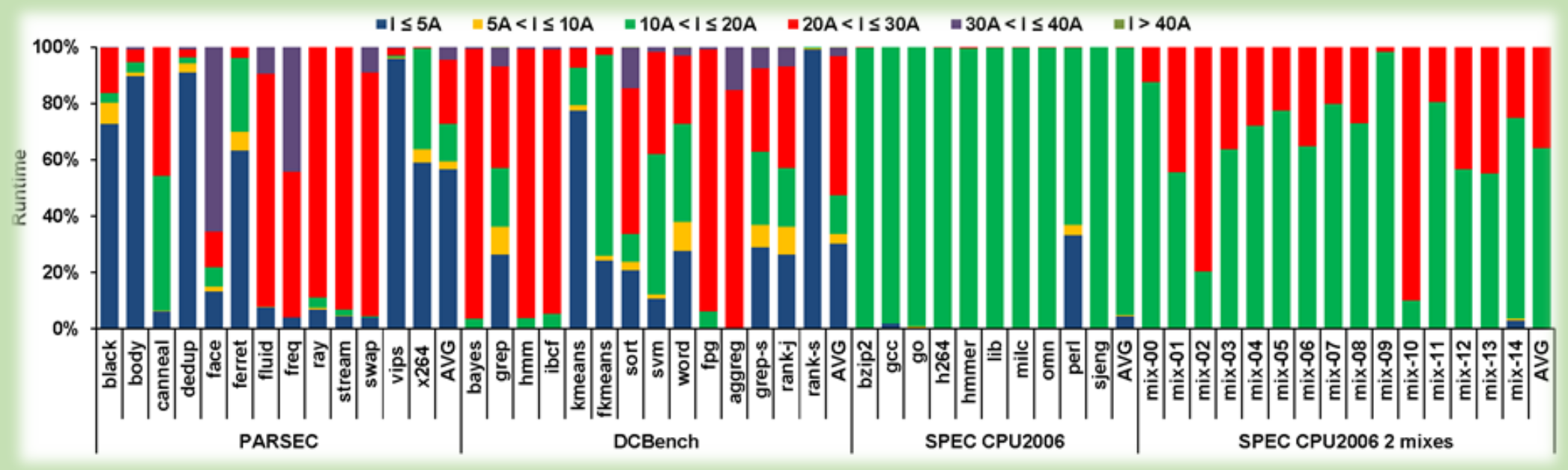
- Voltage regulators consume 22% of total platform power, and occupies 63% more platform area than the processor.
- The frequency of switching transistors on/off determines the output voltage and the current of the system. However, current cannot be increased by just increasing the switching frequency since it will increase the VR switching power loss.
- Multi-phase VRs address this issue by making N phases operate in equally spaced (N x T_{sw}) intervals.



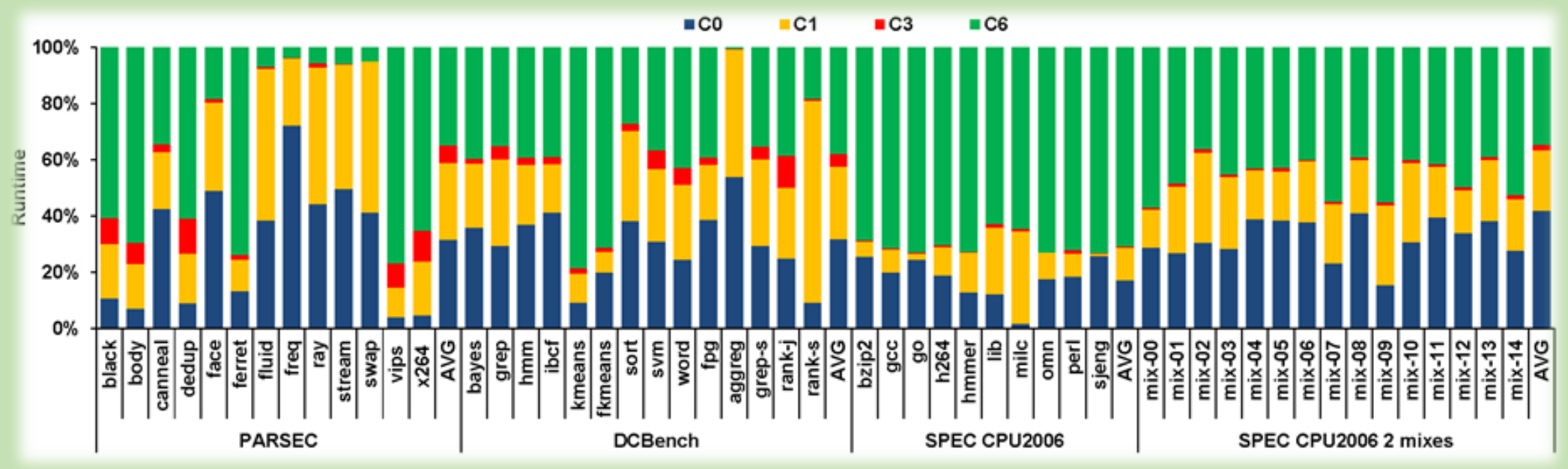
Benchmark Analysis

Our experiments shows that:

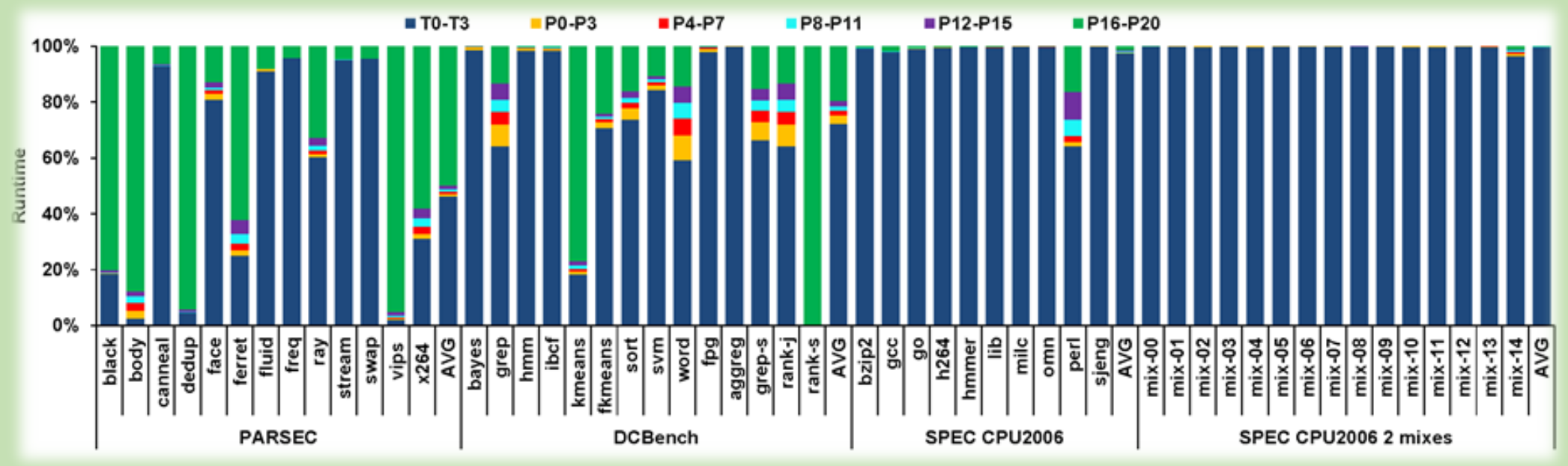
1. The processor consumes low amount of current for most of the time.



2. Cores are in idle-state for a remarkable part of runtime.



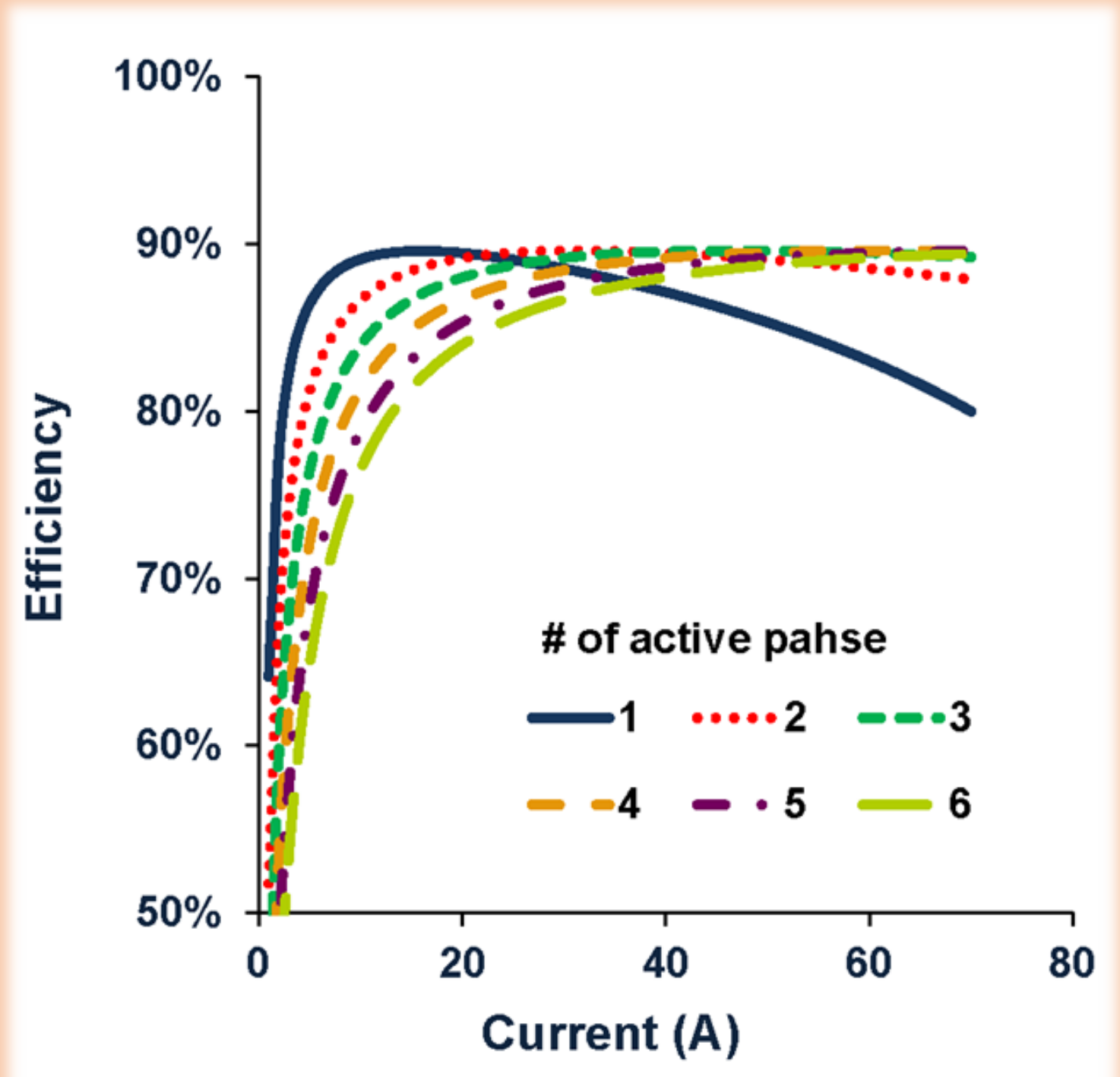
3. More than 50% of the runtime is spent in turbo mode. Therefore, at least one core has high utilization.

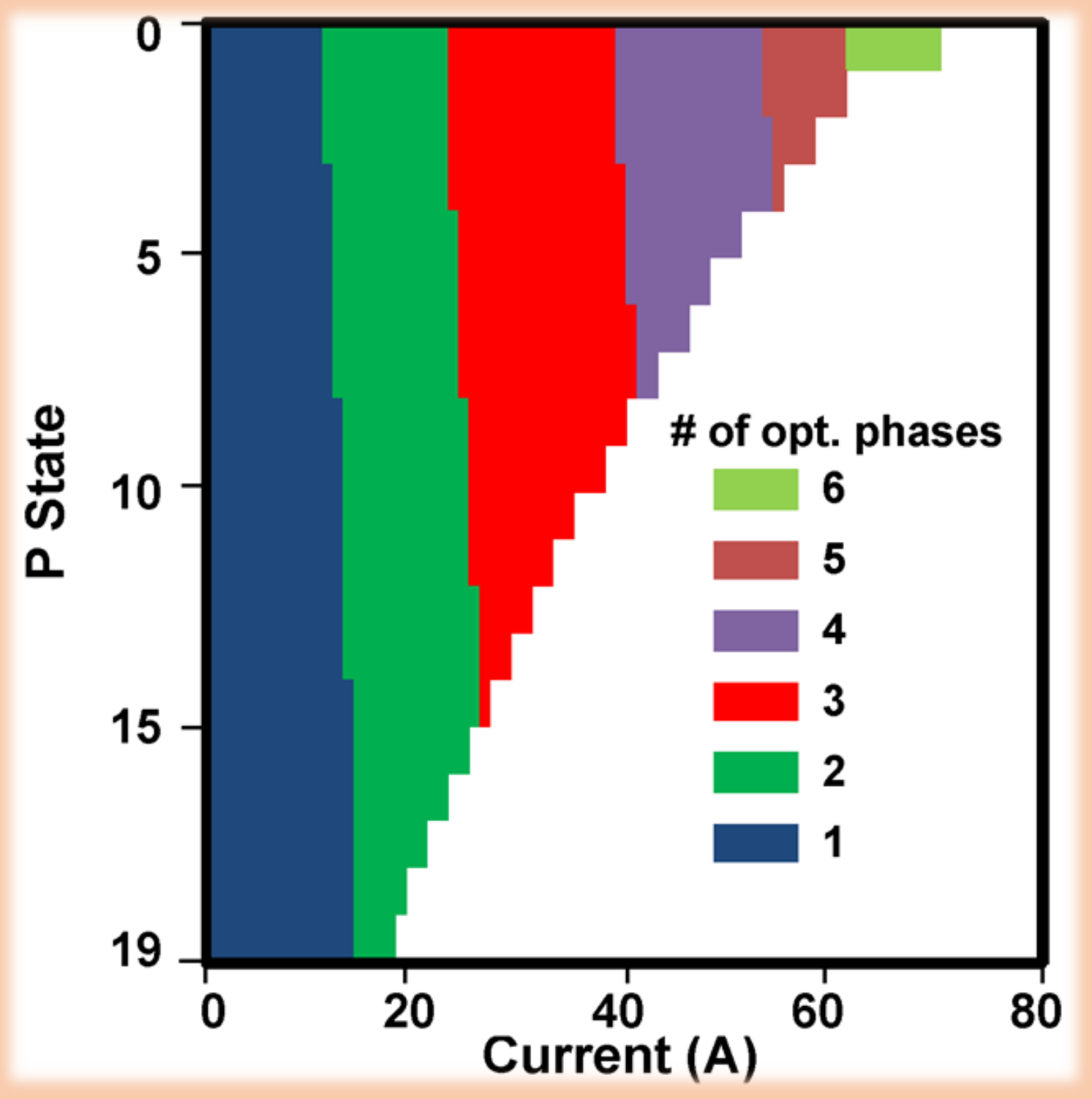


- The experiments show that a significant part of runtime, only one core is active and the rest of the cores are in idle state. Thus, being in turbo mode does not show how large the load current can be and P-state is not a good choice for determining number of active phases based on that.

VR Efficiency

- If we have all the phases active in lower load currents, the switching loss increases and negatively impacts the energy efficiency.
- On the other hand, in higher load currents using multiple phases reduces the conductance loss. Therefore, provides higher efficiency.
- For a load current of 5A, 6 active phases can provide 64% efficiency while having only one active phase can provide as much as 86% efficiency at 1.2 v.
- The maximum current drawn from the voltage regulator is dependent on the P-state of the processor. The optimum number of active phases is determined based on the load current and the P-state.



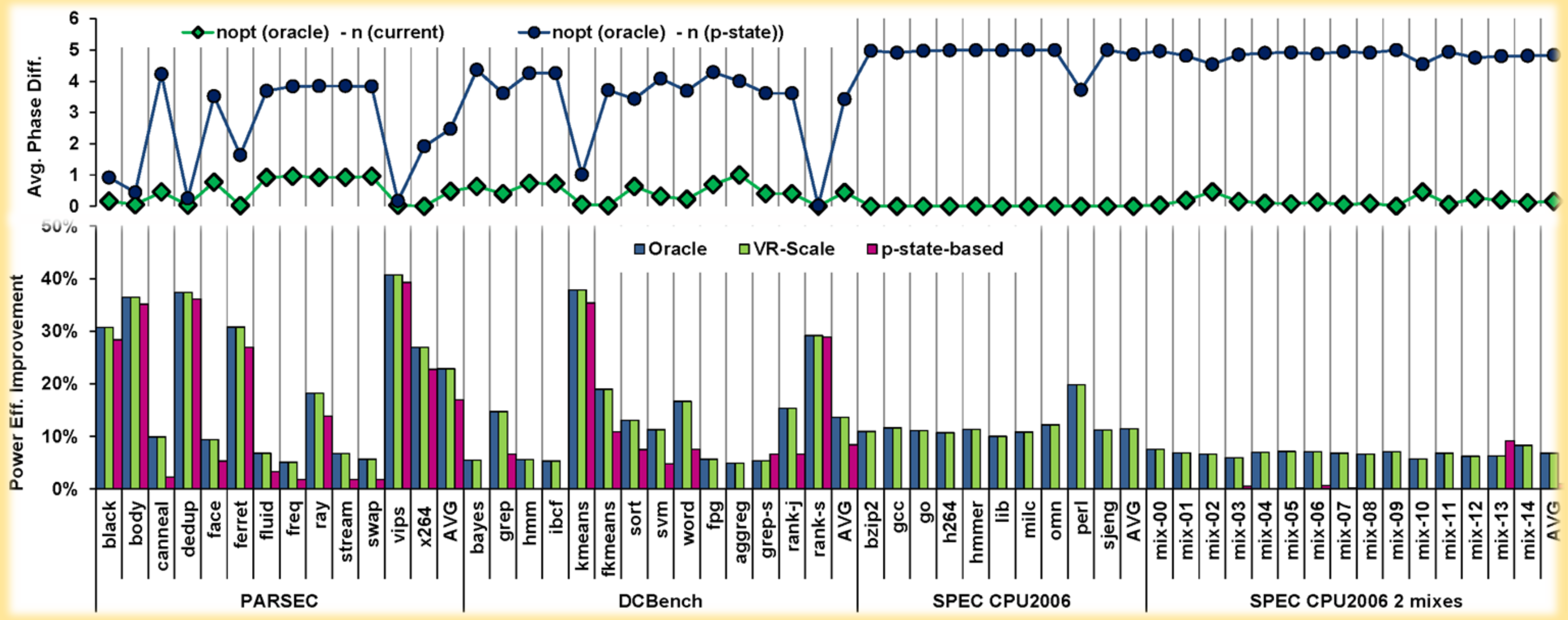


VR-Scale

```
// Algorithm for dynamically scaling number of
// active phases
lut[NUM_PSTATES][NUM_PHASES] = {
{11, 23, 39, 53, 61, 64}, // p_state = 0-3
{12, 24, 40, 53},          // p_state = 4-7
{13, 25, 41, 43},          // p_state = 8-11
{14, 27}};                // p_state = 12-16

int determine_nopt(int p_state, int current){
  nopt = 0;
  while (lut[p_state/4][nopt++] <= current);
    return n;
}
```

- Although, the load current can fluctuate much during the runtime, but in the ms scale the behavior is very predictable.
  - PARSEC: 23% power efficiency improvement with 91% pred accuracy
  - DCBench: 13% power efficiency improvement with 80% pred accuracy
  - SPEC: 11% power efficiency improvement with 99% pred accuracy
- On average, the difference between n_{opt} and n is less than 0.5 for all the benchmarks.


nopt (oracle) - n (current)
nopt (oracle) - n (p-state))
Avg. Phase Diff.
Oracle
VR-Scale
p-state-based
Power Eff. Improvement
black
body
canneal
dedup
face
ferret
fluid
freq
ray
stream
swap
vips
x264
AVG
bayes
grep
hmm
ibcf
kmeans
fkmeans
sort
svm
word
fpg
aggreg
grep-s
rank-j
rank-s
AVG
bzip2
gcc
go
h264
hmmer
lib
milc
omn
perl
sjeng
AVG
mix-00
mix-01
mix-02
mix-03
mix-04
mix-05
mix-06
mix-07
mix-08
mix-09
mix-10
mix-11
mix-12
mix-13
mix-14
AVG
PARSEC
DCBench
SPEC CPU2006
SPEC CPU2006 2 mixes