Hadi Asghari-Moghaddam

4111 Siebel Center,
201 N Goodwin Ave,
Urbana, IL 61801

Phone: (608) 320-8094
Primary Email: asghari2@illinois.edu
Secondary Email: am.hadi@gmail.com

I am a computer architect passionate about designing flexible accelerators for algebra kernels. I have a strong background in designing accelerators in near-data processing and Linux kernel hacking.

Education

Ph.D. Computer Engineering, August 2015 - Present (Expected Graduation Date: May 2021)
University of Illinois at Urbana-Champaign
Current Project: Flexible Tensor Accelerators for Sparse Workloads
Advisor: Christopher Fletcher

M.Sc. Computer Engineering, May 2013 - August 2015
University of Wisconsin Madison
Thesis: Energy Efficient Synchronization Techniques for CMPs
Advisor: Nam Sung Kim

B.Sc. Electrical Engineering, September 2008 - January 2012
Sharif University of Technology
Thesis: A Novel Hardware Implementation for Human Vital Signs Applied to Body Area Networks (BAN)

Selected Publications

- Kartik Hegde, Hadi Asghari-Moghaddam, Michael Pellauer, Neal Crago, Aamer Jaleel, Edgar Solomonik, Joel Emer, Christopher W. Fletcher. "*ExTensor: An Accelerator for Sparse Tensor Algebra.*" IEEE/ACM International Symposium on Microarchitecture **(MICRO)**, 2019.
- Mohammad Alian , Seung Won Min, Hadi Asghari-Moghaddam, Ashutosh Dhar, Dong Kai Wang, Thomas Roewer, Adam McPadden, Oliver OHalloran, Deming Chen, Jinjun Xiong, Daehoon Kim, Wen-mei Hwu, Nam Sung Kim. "*Application-Transparent Near-Memory Processing Architecture with Memory Channel Network.*" IEEE/ACM International Symposium on Microarchitecture **(MICRO)**, 2018.
- Hadi Asghari-Moghaddam, Young Hoon Son, Jung Ho Ahn, and Nam Sung Kim. "*Chameleon: Versatile and practical near-DRAM acceleration architecture for large memory systems.*" IEEE/ACM International Symposium on Microarchitecture **(MICRO)**, 2016.
- Hadi Asghari-Moghaddam, Hamid Reza Ghasemi, Abhishek A. Sinkar, Indrani Paul, and Nam Sung Kim. "*VR-Scale: Runtime Dynamic Phase Scaling of Processor Voltage Regulators for Improving Power Efficiency.*" IEEE/ACM Design Automation Conference **(DAC)**, Jun 2016.
- Hadi Asghari-Moghaddam, Amin Farmahini-Farahani, Katherine Morrow, Jung Ho Ahn, and Nam Sung Kim. "*Near-DRAM Acceleration with Single-ISA Heterogeneous Processing in Standard Memory Modules.*" **IEEE Micro**, 36(1), pp.24-34.
- Hadi Asghari-Moghaddam and Nam Sung Kim. "*SpinWise: A Practical Energy-Efficient Synchronization Technique for CMPs.*" ACM SIGARCH Computer Architecture News 44.1 (2016) 1-8.
- Srinivasan Naraynamoorthy, Hadi Asghari-Moghaddam, Zhenhong Liu, Taejoon Park, and Nam Sung Kim. "*Energy-Efficient Approximate Multiplication for Digital Signal Processing and Classification Applications*" IEEE Transactions on Very Large Scale Integration **(TVLSI)** Systems.

Selected Courses

Computer Architecture: Secure Processor Design (UIUC), Advanced Computer Architecture I & II (Parallel and OoO Core - UW-Madison), Manycore Parallel Algorithms(UIUC), Computer Interfaces, and Computer Architecture & Machine Languages (Sharif University)

Computer Vision & AI: Computer Vision (UIUC), and Artificial Intelligence (UW-Madison)

Operating Systems: Advanced Operating Systems, Operating Systems (UW-Madison), and Distributed Algorithms (UIUC)

FPGA-ASIC: System-On-Chip Design (UIUC), Digital Sys Design & Synthesis, Digital Circuits & Components (UW-Madison), and ASIC/FPGA Chip Design (Sharif University)

Computer Networks & Compilers: Computer Networks (Sharif University), and Programming Languages & Compilers (UIUC)

Skills

- **Programming Languages**: *C/C++ & Python* (OO Programming), *CUDA & MPI* (Parallel Programming), *Haskell* (Functional Programming), *Bash Scripting, Verilog, MATLAB, Java,* and *Assembly* (ARM, MIPS, 8051, x86).
- **Computer Architecture and Kernel Simulators**: *Gem5* (Cycle Accurate Computer System Simulator), *McPAT* (Energy Consumption Estimator), *Qemu* (Kernel Simulator for Kernel Hack Debugging)
- **Hardware Programming Tools**: *Quartus, Modelsim,* and *Design Vision.*
- **Operating Systems**: *Linux* (Extensive Kernel Hacking Experience), *FreeBSD* (Setting-up ZFS, and NFS for iCSL Simulation Cluster), and *Windows*

Selected Academic Projects

∗ *Sparse Accelerators:*

- **Sparse Tensor Accelerators**: Designing flexible tensor accelerators for sparse workloads in a decoupled address execution fashion with dense/sparse pattern genertors. A part of the SDH project in a collaboration with NVIDIA Research, Fall 2018 - Present.

∗ *Near-Data Processing:*

- Designing an **in-storage file system** leveraging near-storage computing capabilities of NVMe SSDs, Spring 2018.
- **Memory Channel Netwok**: Application-Transparent Scale-Out Acceleration Architecture. A Part of the C3SR project in a collaboration with the IBM Watson Research Center, Spring 2016- Fall 2017.
- **Near-DRAM acceleration with single-ISA** heterogeneous processing in standard memory modules, Summer 2015.
- **Near-DRAM acceleration leveraging Load-Reduced DIMM** architecture to improve performance and reduce energy consumption of a system targeting Map-Reduced applications, Spring 2015.

∗ *Hardware Security:*

- **Adversarial Attack on Deep Neural Networks (DNNs)** Circumventing Intel SGX Enclaves Secure Execution Integrity Guarantees, *"Secure Processor Design"* course, Fall 2017.

∗ *Parallel Programming & Profiling*

- **GPU accelerated Bellman-Ford Single-Source Shortest Path (SSSP)** algorithm implementation in GPU, optimized with workfront sweep and near-far pile techniques, *"Manycore Parallel Algorithms"* course, Spring 2017.
- Developing static instrumentation tool for **per-thread performance profiling** of parallel applications, *"Advanced Operating Systems" course*, Fall 2014.
- **Setting-up a simulation cluster** with unified user authentication and storage over more than 500 cores, *"iCSL Research Group"* Fun Experience, Fall 2016.

∗ *Computer Vision*

- **Multi-view vanishing point** extraction for higher accuracy and robust vanishing point detection, *"Computer vision"* course, Spring 2016.

∗ *Hardware Synchronization*

- Design and simulation of **hardware synchronization method** Implicit Queue on Lock Bits **(IQOLB)**, *"Advanced Computer Architecture II" course*, Spring 2015.